REMARKS

In the Final Office Action,[1] the Examiner took the following actions:

> (a) rejected claims 1, 2, 3, 4, 9, 10, 11 and 27-28 under 35 U.S.C. § 103(a) as being unpatentable over Paton et al. (U.S. Patent No. 6,680,250, "*Paton*") in view of Makovicka et al. (U.S. Patent Publication No. 2004/0224470, "*Makovicka*"); and
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> (b) rejected claims 5, 7, 8, 12, 14-15, 25-26 and 29-30 under 35 U.S.C. § 103(a) as being unpatentable over *Paton* in view of *Makovicka* and further in view of Arai et al. (U.S. Patent No. 4,504,323, "*Arai*") and Timans et al. (U.S. Patent No. 6,951,996, "*Timans*").

Claims 6 and 13 were previously canceled and claims 16-24 stand withdrawn. Claims 1-5, 7-12, 14-15, and 25-34 are currently under examination.

At the onset, Applicant notes that Final Office Action does not discuss claims 31-34. Applicant therefore presumes that these claims are allowed. Should the Examiner continue to dispute the patentability of claims 31-34, however, Applicant requests that the Examiner withdrawn the finality of the pending Office Action and clearly articulate the basis of his rejection in another, non-final Office Action in order to provide Applicant the opportunity to respond to any contentions raised by the Examiner.

Applicant respectfully traverses the rejection of claims 1, 2, 3, 4, 9, 10, 11 and 27-28 under 35 U.S.C. § 103(a) as being unpatentable over *Paton* in view of *Makovicka*. No *prima facie* case of obviousness is established.

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[1] The Final Office Action contains statements reflecting characterizations of the related art and the claims. Regardless of whether any such statement is identified herein, Applicant declines to automatically subscribe to any statement or characterization in the Office Action.

The key to supporting any rejection under 35 U.S.C. § 103 is the clear articulation of the reason(s) why the claimed invention would have been obvious. Such an analysis should be made explicit and cannot be premised upon mere conclusory statements. M.P.E.P. § 2142, 8th Ed., Rev. 6 (Sept. 2007). "A conclusion of obviousness requires that the reference(s) relied upon be enabling in that it put the public in possession of the claimed invention." M.P.E.P. § 2145. Furthermore, "[t]he mere fact that references can be combined or modified does not render the resultant combination obvious unless the results would have been predictable to one of ordinary skill in the art" at the time the invention was made. M.P.E.P. § 2143.01(III), internal citation omitted. Moreover, "[i]n determining the differences between the prior art and the claims, the question under 35 U.S.C. § 103 is not whether the differences *themselves* would have been obvious, but whether the claimed invention *as a whole* would have been obvious." M.P.E.P. § 2141.02(I), internal citations omitted (emphasis in original).

"[T]he framework for the objective analysis for determining obviousness under 35 U.S.C. 103 is stated in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). ... The factual inquiries...[include determining the scope and content of the prior art and]...[a]scertaining the differences between the claimed invention and the prior art." M.P.E.P. § 2141(II). "Office personnel must explain why the difference(s) between the prior art and the claimed invention would have been obvious to one of ordinary skill in the art." M.P.E.P. § 2141(III).

Claim 1 recites, *inter alia*, "implanting an electrically inactive first impurity over substantially one entire side of a semiconductor substrate . . . wherein the first impurity

is implanted . . . [in] a semiconductor element forming region . . . including the gate electrode, and an upper portion of an isolation region." The Examiner acknowledges that *Paton* fails to depict isolation regions. Final Office Action at 4. Nevertheless, the Examiner contends that it would be obvious to reproduce the process disclosed by *Paton* and "include forming the obviously required isolations regions . . . [and thus] it is obvious that the first impurity would be implanted into the isolation structure along with all of the other features that are exposed on/in the surface of the substrate." *Id.*

The Examiner then points to *Makovicka* as allegedly teaching a means to mitigate transient enhanced diffusion (TED), which the Examiner appears to associate with the claimed "first impurity . . . implanted into a semiconductor element forming region formed in the surface layer of the semiconductor substrate including the gate electrode, and an upper portion of an isolation region formed in the surface layer of the semiconductor substrate," as recited in claim 1. *Id.* at 5. The Examiner's conclusions are incorrect for at least the reasons discussed below.

First, the Examiner has not pointed out which elements of *Paton* and *Makovicka* allegedly correspond to the claimed "first impurity . . . implanted . . . [in] a semiconductor element forming region . . . including the gate electrode, and an upper portion of an isolation region ," as recited in claim 1. Instead, the Examiner merely contends that isolation regions are "conventionally formed prior to forming the gates and implanting." *Id.* at 4. The Examiner concludes on this basis that the combination of elements is obvious because one of ordinary skill would have been motivated to look at other methods of "performing the disclosed isolation region forming step of *Paton*." *Id.* at 5.

As discussed above, the Examiner acknowledges that *Paton* fails to depict isolation regions. *Makovicka* is silent on the claimed "first impurity . . . implanted . . . [in] a semiconductor element forming region . . . including the gate electrode, and an upper portion of an isolation region." *Makovicka*, therefore, cannot cure the deficiencies of *Paton*. Accordingly, the Examiner's proposed combination fails to teach or suggest at least the claimed "implanting an electrically inactive first impurity *over substantially one entire side of a semiconductor substrate* . . . wherein the first impurity is implanted . . . [in] a semiconductor element forming region . . . *including the gate electrode, and an upper portion of an isolation region*," as recited in claim 1 and, thus, the proposed combination fails to teach or suggest each and every element recited in claim 1 (emphasis added). No *prima facie* case of obviousness is established for at least this reason.

Second, even assuming *arguendo* that *Makovicka* did provide teachings consistent with the Examiner's position, the method in *Makovicka* that the Examiner cites produces either "undesirabl[e] results" or at a minimum, "localize[d] . . . damage to the surface regions of the substrate." *Makovicka*, para. [0006]. *Makovicka*, thus, teaches away from the Examiner's proposed combination and one of ordinary skill in the art would not combine the references in the Examiner's proposed manner for at least this reason.

In view of the above deficiencies of the cited references, the Final Office Action has neither properly determined the scope and content of the prior art nor properly ascertained the differences between the prior art and the claimed invention. Accordingly, no reason has been clearly articulated as to why claim 1 would have been

obvious to one of ordinary skill in view of the prior art. Claim 1, therefore, should be allowable.

Moreover, independent claim 9, although of different scope, recited similar elements as claim 1 and should be allowable for at least the same reasons as claim 1. Claims 2, 3, 4, 10, 11, 27 and 28 depend from claim 1 or 9 and should be allowable at least due to their dependence. Accordingly, Applicant requests that the Examiner reconsider and withdraw the rejections of claims 1, 2, 3, 4, 9, 10, 11 and 27-28 under 35 U.S.C. § 103(a).

In addition to the reasons discussed above, in an exemplary embodiment discussed at page 9, line 21, p-well and n-well layers are formed on nMOS and pMOS regions (i.e., a CMOS transistor). As illustrated in that exemplary embodiment, an electrically inactive impurity is ion-implanted into the upper portion of each gate electrode and surface layer of the silicon substrate. Such an exemplary embodiment is not contemplated by the combination of *Paton* and *Makovicka* for similar reasons as those discussed above.

Applicant respectfully traverses the rejections of claims 5, 7, 8, 12, 14-15, 25-26 and 29-30 under 35 U.S.C. § 103(a) as being unpatentable over *Paton* in view of *Makovicka* and further in view of *Arai* and *Timans*. No *prima facie* case of obviousness is established.

Claims 5, 7, 8, 12, 14-15, 25-26 and 29-30 depend from independent claims 1, 9, 25, or 26 and thus incorporate each and every element of their respective independent claim. *Paton* and *Makovicka* fail to teach or suggest "implanting an electrically inactive first impurity over substantially one entire side of a semiconductor substrate . . . wherein

the first impurity is implanted . . . [in] a semiconductor element forming region . . . including the gate electrode, and an upper portion of an isolation region," as recited in claim 1, or similar element recited in claims 9, 25, and 26, for at least the reasons above.

Arai and *Timans* fail to cure the deficiencies of *Paton* and *Makovicka*. *Arai* discloses "equipment and a method for annealing semiconductors." Col. 1, lines 11-12. *Timans* discloses "methods and systems for heat-treating semiconductor wafers with short, high-intensity pulses, in combination with background heating sources." Col. 1, lines 14-17. Neither *Arai* nor *Timans*, however, teach or suggest the claimed "isolation region," recited in claim 1 (or similar elements of claims 9, 25, and 26) and required by claims 5, 7, 8, 12, 14-15, 25-26 and 29-30 due to their dependence. In addition, neither *Aria* and *Timans* remedy the teaching away from the Examiner's proposed combination due to the aspects *Makovicka* method discussed above.

For at least the above discussed reasons, the Final Office Action has neither properly determined the scope and content of the prior art nor properly ascertained the differences between the prior art and the claimed invention. Accordingly, no reason has been clearly articulated as to why claims 1, 9, 25, and 26 would have been obvious to one of ordinary skill in view of the prior art. Therefore, a *prima facie* case of obviousness has not been established for claims 5, 7, 8, 12, 14-15, 25-26 and 29-30 at least due to their dependence from claims 1, 9, 25, and 26. Accordingly, Applicant respectfully requests that the Examiner reconsider and withdraw the rejection of claim 5, 7, 8, 12, 14-15, 25-26 and 29-30 under § 103.

Claims 31-34 are allowable at least due to their dependence. Moreover, as noted above, Applicant assumes claims 31-34 to be allowed in the absence of clarification from the Examiner to the contrary. Thus, claims 1-5, 7-12, 14-15, and 25-34 are in condition for allowance.

In view of the foregoing, Applicant respectfully requests reconsideration and reexamination of this application and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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